WHAT IS CLAIMED IS:

1. A pattern layout method of a semiconductor made in one chip with an anode driver, a cathode driver, and memory portions comprising the steps of:

laying out drivers connected to the memory portions equally in the chip; and

arranging each memory portion equally in the vicinity of each of the drivers.

2. The pattern layout method of a semiconductor device according to claim 1, wherein the desired drivers connected to the memory portions are divided into plural groups and each of the memory portions is arranged in every group.

3. The pattern layout method of a semiconductor device according to claim 1, wherein the drivers connected to the memory portions are placed face to face at right and left positions or high and low positions, and each memory portion is arranged at center portion of the chip.

4. The pattern layout method of a semiconductor device according to claim 1, wherein each of the drivers includes a plurality of output regions corresponding to one bit constituting an output bit group, the method further comprising

the step of forming a dummy pattern having the same shape as the output bit to be adjacent to the end portion of the output bit group.

5. The pattern layout method of a semiconductor device according to claim 4, wherein the dummy pattern is formed at an empty space in a region where a plurality of output bits are arranged.

6. The pattern layout method of a semiconductor device according to claim 4, wherein number of outputs of the dummy pattern formed at a region where output bit groups are adjacent each other is less than number of outputs of the dummy pattern formed at a region where output bit groups are not adjacent each other.

7. The pattern layout method of a semiconductor device according to claim 4, wherein the dummy pattern has the same shape as a wiring for gate electrode.

8. A pattern layout method of a semiconductor device for drivers where plural output regions corresponding to one bit are arranged to constitute desired output bit group and made in one chip comprising the step of:

arranging a plurality of the output group at periphery

portion in the chip.

9. The pattern layout method of a semiconductor device according to claim 8, further comprising the step of:

arranging wirings connected to each of the output bit groups arranged at the periphery portion to circle fitting shape of the chip.

10. A pattern layout method of a semiconductor device constituting drivers for driving display where drivers, memory portions are made in one chip, the drivers arranging plural output regions corresponding to one bit to constitute output bit groups, the method comprising the steps of:

arranging the drivers at periphery portion in the chip in the state of grouping by every desired output bit group; and

arranging wirings connected to each output bit arranged at the periphery portion to circle fitting shape of the chip.

11. The pattern layout method of a semiconductor device according to claim 10,

wherein the drivers includes an anode driver and a cathode driver, and the drivers are arranged at periphery portion in the chip in a state that one of the anode driver and the cathode driver is grouped by every desired output bit group.

12. The pattern layout method of a semiconductor device according to claim 10, wherein the wiring includes a power source line and a signal line.

13. The pattern layout method of a semiconductor device according to claim 10 wherein the each of the output bit group is arranged to surround the memory portions at the periphery portion.

14. The pattern layout method of a semiconductor device according to claim 10, further comprising the step of forming a dummy pattern having the same shape as the output bit to be adjacent to the end portion of the output bit group.

15. The pattern layout method of a semiconductor device according to claim 14, wherein the dummy pattern is formed at an empty space in a region where a plurality of output bits are arranged.

16. The pattern layout method of a semiconductor device according to claim 14, wherein number of outputs of the dummy pattern formed at a region where output bit groups are adjacent each other is less than number of outputs of the dummy pattern formed at a region where output bit groups are not adjacent

each other.

17. The pattern layout method of a semiconductor device according to claim 14, wherein the dummy pattern has the same shape as a wiring for gate electrode.